What Is Claimed Is:

1. A memory array comprising:

a first row of transistors and a second row of transistors being located in adjacent rows;

a first word line connected to each of said first row of transistors; and

a second word line connected to each of said second row of transistors,

wherein a layer forming said first word line is laid on top of a layer forming said second word line in a layout forming said memory array.

2. The memory array of claim 1, wherein each of said first row of transistors and said second row of transistors comprises:

a diffusion layer forming a drain area and a source area;

a poly-silicon layer forming a gate area for said first row of transistors and said second row of transistors; and

a metal1 layer forming said first word line.

3. The memory array of claim 2, further comprising a metal2 layer forming said second word line.

4. The memory array of claim 3, further comprising a metal3 layer forming a plurality of bit lines.

5. The memory array of claim 4, further comprising a contact layer to connect said

metal1 layer to said poly-silicon layer forming said gate area of said first row of transistors.

6. The memory array of claim 5, further comprising a Via1 layer, wherein said Via1 layer and said contact layer connect said metal2 layer to said poly-silicon layer forming said gate area of said second row of transistors.

7. The memory array of claim 6, further comprising a plurality of metal islands formed by said metal1 layer, said metal2 layer, said metal3 layer, said Via1 layer and said contact layer.

8. The memory array of claim 7, wherein a Via2 layer is used with each of said plurality of metal islands to program a corresponding bit cell to either 0 or 1.

9. The memory array of claim 8, further comprising a power strap formed by said metal1 layer, said metal2 layer, said metal3 layer, said Via1 layer, said Via2 layer, and said contact layer, wherein said contact layer connects Vss to said source area of each of said first row of transistors and said second row of transistors.

10. The memory array of claim 2, further comprising a metal3 layer forming said second word line.

11. The memory array of claim 10, further comprising a metal2 layer forming a plurality of bit lines.

12. The memory array of claim 11, further comprising a contact layer to connect said metal1 layer to said poly-silicon layer forming said gate area of said first row of transistors.

13. The memory array of claim 12, further comprising a Via1 layer and a Via2 layer, wherein said Via1 layer, said Via2 layer and said contact layer connect said metal3 layer to said poly-silicon layer forming said gate area of said second row of transistors.

14. The memory array of claim 13, further comprising a plurality of metal islands formed by said metal1 layer, said metal2 layer, said metal3 layer, said Via1 layer and said contact layer.

15. The memory array of claim 7, wherein a Via1 layer is used with each of said plurality of metal islands to program a corresponding bit cell to either 0 or 1.

16. The memory array of claim 8, further comprising a power strap formed by said metal1 layer, said metal2 layer, said metal3 layer, said Via1 layer, said Via2 layer, and said contact layer, wherein said contact layer connects Vss to said source area of each of said first row of transistors and said second row of transistors.

17. A memory unit comprising:

a memory array comprising:

a first row of transistors and a second row of transistors being located

in adjacent rows, wherein each of said first row of transistors and said second row of transistors is designed to store a bit value;

a first word line connected to each of said first row of transistors; and

a second word line connected to each of said second row of transistors, wherein a layer forming said first word line is laid on top of a layer forming said second word line in a layout forming said memory array;

a decoder circuit receiving an address identifying one of said first row of transistors and said second row of transistors, and retrieving said bit value stored in the transistor identified by said address.

18. The memory unit of claim 17, wherein each of said first row of transistors and said second row of transistors comprises:

a diffusion layer forming a drain area and a source area;

a poly-silicon layer forming a gate area for said first row of transistors and said second row of transistors; and

a metal1 layer forming said first word line.

19. The memory unit of claim 18, further comprising a metal2 layer forming said second word line.

20. The memory unit of claim 19, further comprising a metal3 layer forming a plurality of bit lines.

21. The memory unit of claim 20, further comprising a contact layer to connect said metal1 layer to said poly-silicon layer forming said gate area of said first row of transistors.

22. The memory unit of claim 21, further comprising a Via1 layer, wherein said Via1 layer and said contact layer connect said metal2 layer to said poly-silicon layer forming said gate area of said second row of transistors.

23. The memory unit of claim 22, further comprising a plurality of metal islands formed by said metal1 layer, said metal2 layer, said metal3 layer, said Via1 layer and said contact layer.

24. The memory unit of claim 23, wherein a Via2 layer is used with each of said plurality of metal islands to program a corresponding bit cell to either 0 or 1.

25. The memory unit of claim 24, further comprising a power strap formed by said metal1 layer, said metal2 layer, said metal3 layer, said Via1 layer, said Via2 layer, and said contact layer, wherein said contact layer connects Vss to said source area of each of said first row of transistors and said second row of transistors.

26. The memory unit of claim 18, further comprising a metal3 layer forming said second word line.

27. The memory unit of claim 26, further comprising a metal2 layer forming a

plurality of bit lines.

28. The memory unit of claim 27, further comprising a contact layer to connect said metal1 layer to said poly-silicon layer forming said gate area of said first row of transistors.

29. The memory unit of claim 28, further comprising a Via1 layer and a Via2 layer, wherein said Via1 layer, said Via2 layer and said contact layer connect said metal3 layer to said poly-silicon layer forming said gate area of said second row of transistors.

30. The memory unit of claim 29, further comprising a plurality of metal islands formed by said metal1 layer, said metal2 layer, said metal3 layer, said Via1 layer and said contact layer.

31. The memory unit of claim 23, wherein a Via1 layer is used with each of said plurality of metal islands to program a corresponding bit cell to either 0 or 1.

32. The memory unit of claim 24, further comprising a power strap formed by said metal1 layer, said metal2 layer, said metal3 layer, said Via1 layer, said Via2 layer, and said contact layer, wherein said contact layer connects Vss to said source area of each of said first row of transistors and said second row of transistors.

33. The memory unit of claim 32, wherein said memory unit represents a ROM.

34. A device comprising:

a memory array comprising:

a first row of transistors and a second row of transistors being located in adjacent rows, wherein each of said first row of transistors and said second row of transistors is designed to store a bit value;

a first word line connected to each of said first row of transistors; and

a second word line connected to each of said second row of transistors,

wherein a layer forming said first word line is laid on top of a layer forming said second word line in a layout forming said memory array;

a decoder circuit receiving an address identifying one of said first row of transistors and said second row of transistors, and retrieving said bit value stored in the transistor identified by said address; and

a processing unit receiving said bit value.

35. The device of claim 34, wherein each of said first row of transistors and said second row of transistors comprises:

a diffusion layer forming a drain area and a source area;

a poly-silicon layer forming a gate area for said first row of transistors and said second row of transistors; and

a metal1 layer forming said first word line.

36. The device of claim 35, further comprising a metal2 layer forming said second word line.

37. The device of claim 36, further comprising a metal3 layer forming a plurality of bit lines.

38. The device of claim 37, further comprising a contact layer to connect said metal1 layer to said poly-silicon layer forming said gate area of said first row of transistors.

39. The device of claim 38, further comprising a Via1 layer, wherein said Via1 layer and said contact layer connect said metal2 layer to said poly-silicon layer forming said gate area of said second row of transistors.

40. The device of claim 39, further comprising a plurality of metal islands formed by said metal1 layer, said metal2 layer, said metal3 layer, said Via1 layer and said contact layer.

41. The device of claim 40, wherein a Via2 layer is used with each of said plurality of metal islands to program a corresponding bit cell to either 0 or 1.

42. The device of claim 41, further comprising a power strap formed by said metal1 layer, said metal2 layer, said metal3 layer, said Via1 layer, said Via2 layer, and said contact layer, wherein said contact layer connects Vss to said source area of each of said first row of transistors and said second row of transistors.

43. The device of claim 35, further comprising a metal3 layer forming said second

word line.

44. The device of claim 43, further comprising a metal2 layer forming a plurality of bit lines.

45. The device of claim 44, further comprising a contact layer to connect said metal1 layer to said poly-silicon layer forming said gate area of said first row of transistors.

46. The device of claim 45, further comprising a Via1 layer and a Via2 layer, wherein said Via1 layer, said Via2 layer and said contact layer connect said metal3 layer to said poly-silicon layer forming said gate area of said second row of transistors.

47. The device of claim 46, further comprising a plurality of metal islands formed by said metal1 layer, said metal2 layer, said metal3 layer, said Via1 layer and said contact layer.

48. The device of claim 40, wherein a Via1 layer is used with each of said plurality of metal islands to program a corresponding bit cell to either 0 or 1.

49. The device of claim 41, further comprising a power strap formed by said metal1 layer, said metal2 layer, said metal3 layer, said Via1 layer, said Via2 layer, and said contact layer, wherein said contact layer connects Vss to said source area of each of said first row of transistors and said second row of transistors.

50. A method of manufacturing a memory array containing a first row of transistors, a second row of transistors, a first word line and a second word line, wherein said first word line is coupled to each of said first row of transistors and said second word line is coupled to each of said second row of transistors, said method comprising:

laying a first layer representing said first word line; and

laying a second layer representing said second word line, wherein said second layer is laid on top of said first layer.

51. The method of claim 50, further comprising:

implanting a diffusion layer in a substrate to form a source area and a drain area corresponding to each of said first row of transistors and said second row of transistors;

depositing a first poly-silicon layer to form a gate area corresponding to each of said first row of transistors;

depositing a second poly-silicon layer to form a gate area corresponding to each of said second row of transistors; and

laying via layers to connect said first poly-silicon layer to said first layer, and said second poly-silicon layer to said second layer;

52. The method of claim 51, wherein said first layer is formed by a metal1 layer and said second layer is formed by a metal2 layer.

53. The method of claim 52, further comprising:

depositing metal3 layer to form a plurality of bit lines and a plurality of metal islands,

wherein each of plurality of metal islands is also formed by said metal1 layer and said metal2 layer.

54. The method of claim 53, further comprising:

laying a plurality of contact layers to connect said diffusion layer to each of said plurality of metal islands, and said metal1 layer to each of said first poly-silicon layer and second poly-silicon layer.

55. The method of claim 54, further comprising:

laying via2 layer only in some of said plurality of metal islands requiring programming of a first logical value.

56. The method of claim 51, wherein said first layer is formed by a metal1 layer and said second layer is formed by a metal3 layer.

57. The method of claim 56, further comprising:

depositing metal2 layer to form a plurality of bit lines and a plurality of metal islands, wherein each of plurality of metal islands is also formed by said metal1 layer and said metal3 layer.

58. The method of claim 57, further comprising:

laying a plurality of contact layers to connect said diffusion layer to each of said plurality of metal islands, and said metal1 layer to each of said first poly-silicon layer and

second poly-silicon layer.

59. The method of claim 58, further comprising:

laying via1 layer only in some of said plurality of metal islands requiring programming of a first logical value.